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## NOTICE OF ALLOWANCE AND FEE(S) DUE

79184

7590

10/20/2008

HANIFY & KING PROFESSIONAL CORPORATION  
1875 K STREET, NW  
SUITE 707  
WASHINGTON, DC 20006

EXAMINER

NAM, HYUN

ART UNIT

PAPER NUMBER

2184

DATE MAILED: 10/20/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,958	05/21/2004	Hiroshi Takahashi	5243-006-US01	8037

TITLE OF INVENTION: OPERATION MODE CONTROL CIRCUIT, MICROCOMPUTER INCLUDING THE SAME, AND CONTROL SYSTEM  
USING THE MICROCOMPUTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	01/20/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE** OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

## HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER:** Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

# **PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to:** **Mail** **Mail Stop ISSUE FEE**  
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**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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79184 7590 10/20/2008

**HANIFY & KING PROFESSIONAL CORPORATION**  
**1875 K STREET, NW**  
**SUITE 707**  
**WASHINGTON, DC 20006**

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/84/958 05/21/2004

Hitoshi Takahashi

5243-006-U001

8037

**TITLE OF INVENTION: OPERATION MODE CONTROL CIRCUIT, MICROCOMPUTER INCLUDING THE SAME, AND CONTROL SYSTEM USING THE MICROCOMPUTER**

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	01/20/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
NAM, HYUN	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_  
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_  
3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee  
☐ Publication Fee (No small entity discount permitted)  
☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.  
☐ Payment by credit card. Form PTO-2038 is attached.  
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature \_\_\_\_\_ Date \_\_\_\_\_  
Typed or printed name \_\_\_\_\_ Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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10/849,958	05/21/2004	Hitoshi Takahashi	5243-006-US01	8037
79184	7590	10/20/2008	EXAMINER	
HANIFY & KING PROFESSIONAL CORPORATION 1875 K STREET, NW SUITE 707 WASHINGTON, DC 20006			NAM, HYUN	
			ART UNIT	PAPER NUMBER
			2184	
DATE MAILED: 10/20/2008				

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 542 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 542 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

**Notice of Allowability****Application No.**

10/849,958

**Examiner**

Hyun Nam

**Applicant(s)**

TAKAHASHI, HITOSHI

**Art Unit**

2184

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/3/2008.
2. ☒ The allowed claim(s) is/are 4, 5, 10, and 13-16.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some\* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date 10/3/2008
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_.

/Henry W.H. Tsai/  
Supervisory Patent Examiner, Art Unit 2184

## DETAILED ACTION

### *Allowable Subject Matter*

Claims 4, 5, 10, and 13-16 (renumbered as 1- 7 respectively) are allowed. The following is an examiner's statement of reasons for allowance the prior art does not teach or fairly suggest in renumbered claims 1-7:

Claim 4 recites - wherein the write protection circuit comprises:

buffer units for outputting a buffer signal that is a buffered version of a first signal of the first output signal and outputting a fixed logical value signal in response to the first output signal excluding the first signal of the first output signal output from the control signal generator; and

latch units for performing a latch process in response to the first output signal from the control signal generator and for outputting a status signal indicating a latch status thereof,

wherein the buffer units has an input terminal for receiving the status signal from the latch units, and outputs the fixed logical value signal if the status signal indicates the latch status, or outputs the buffer signal if the status signal does not indicate the latch status

Claim 5 recites - wherein the write protection circuit comprises:

an AND gate for receiving the first output signal from the control signal generator at one of input terminals thereof;

a flip-flop, with a reset terminal and a clock terminal thereof connected to an output terminal of the AND gate, for outputting a signal having a logical signal "0" when the reset signal is received at the reset terminal and for outputting a signal having a logical signal "1" when a pulse signal is received at the clock terminal thereof; and

a buffer for outputting a logically inverted version of a signal from the flip-flop to the other of the input terminals of the AND gate,

wherein the AND gate AND gates the first output signal from the control signal generator and the logically inverted version of the signal from the flip-flop

Claim 10 recites - wherein the write protection circuit comprises:

a decoder for outputting a first selection status signal and a second selection status signal in response to the first decode signal and the second decode signal from the control signal generator, respectively;

a first AND gate for receiving the first selection status signal at one of input terminals thereof;

a second AND gate for receiving the second selection status signal at one of input terminals thereof;

a third AND gate;

a first flip-flop for latching an output signal from the first AND gate in response to the first output signal from the control signal generator and for outputting first data to the other of the input terminals of the second AND gate;

a second flip-flop for latching an output from the second AND gate in response to the first output signal from the control signal generator and for outputting second data to one of input terminals of the third AND gate; and a buffer for outputting, to the other of the input terminals of the first AND gate, a third output signal that is a logically inverted version of the second data.

wherein the first AND gate AND gates the first election status signal and the third output signal,

wherein the second AND gate AND gates the second selection status signal and the first data,

wherein the third AND gate AND gates the second data and the first output signal, and

wherein the control circuit includes a third flip-flop that latches the second output signal from the control signal generator in response to an output signal from the third AND gate

Claim 13 recites - a second control circuit for latching a fifth output signal from the control signal generator in response to a fourth output signal from the control signal generator, and for generating a second control signal responsive to a logical value of the fifth output signal latched in the second control circuit; and  
an OR gate for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal



Claim 14 recites – wherein the write protection circuit comprises:

buffer units for outputting one of the buffer signal resulting from the first output signal and the signal having the fixed logical value in response to the first output signal from the control signal generator, and latch units for latching the second output signal from the control signal generator in response to the buffer signal and outputting a logical signal responsive to the logical value of the second output signal,

wherein the buffer units receives the logical signal from the latch units, and outputs a signal with the logical value thereof fixed in response to one logical value of the logical signal while outputting the buffer signal in response to the other logical value of the logical signal

Claim 15 recites – wherein the write protection circuit comprises:

an AND gate for receiving, at one of input terminals thereof, the first output signal from the control signal generator;

a buffer for outputting a buffer signal that is an logically inverted version of the second output signal from the control signal generator; and a latch for receiving the buffer signal at a data terminal thereof, for latching the buffer

Art Unit: 2184

signal in response to an output from the AND gate, and for generating a logical signal responsive to the logical value of the buffer signal,

wherein the AND gate AND gates the logical signal and the first output signal

Claim 16 recites - a second control circuit for latching a fifth output signal from the control signal generator in response to a fourth output signal from the control signal generator, and for generating a second control signal responsive to the logical value of the latched fifth output signal, and an OR gate for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal.

Further, the combination of the set forth limitations with all of the other limitations in the respective independent claims (renumbered claims 1-7) are not obvious.

Applicant has argued these limitations on pages 16 and 19, of Applicant's Remarks filed 10-4-2007. This limitation finds support in the specification on pages 8-11. The prior art of record neither anticipates nor renders obvious the above recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled

Art Unit: 2184

"Comments on Statement of Reasons for Allowance."

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hyun Nam whose telephone number is (571) 270-1725. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Henry W.H. Tsai/  
Supervisory Patent Examiner, Art Unit 2184